Attorney Ref: 3175-Z

AFW
AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of
Laung-Terng Wang et al.
Application No. 10/086,214
Filed: March 27, 2002
For: METHOD AND APPARATUS FOR DIAGNOSING FAILURES IN AN INTEGRATED CIRCUIT USING DESIGN-for-DEBUG (DFD) TECHNIQUES

Examiner James C. Kerveros
Group Art Unit 2133

TRANSMITTAL FOR AMENDED BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached hereto is an AMENDED BRIEF ON APPEAL for the above-identified application which is in compliance with 37 C.F.R. 41.37.

Insofar as the three points noted by the Patent Appeals Specialist, Item 1 has been corrected to show a heading reading: SUMMARY OF CLAIMED SUBJECT MATTER.

As to Item 4, the appeal brief originally filed does describe independent claim 85. See page 3, bottom line; page 7, second and third full paragraphs; page 8, first full paragraph. Each claim is treated independently throughout the rest of the brief.

Insofar as Item 6 is concerned, appellants are not required to rely on any citation of case authority. And the statutes relied on are cited as 35 U.S.C. 102 and 103. The parts of the record relied on are in appellants' patent specification which are cited and referenced at different pages of the brief. The references cited by the Examiner in the rejection have been identified and portions thereof which appellants refer to have been cited by column and line numbers. For example, at page 8 of appellants' brief, portions of the Swamy reference are cited and referred to by column and line number.

Note also that the brief contains arguments under separate headings for each ground as follows:

"Ground No. 1", page 6,
"Ground No. 2", page 9,
"Ground No. 3", page 10, and
"Ground No. 4", page 10.

In addition to changing the title of Part V. on page 2, the following additional changes have been entered to the brief: At page 6, under Ground No. 1, line 2, "85" has been inserted after "claim". At the end of the page, the quote from the Examiner's final rejection has been identified as page 3, of the Final Rejection.

In the first full paragraph on page 7, the quotation in the Swamy reference has been identified as column 7, lines 17 *et seq.*

The payment of the brief fee was made with the earlier filed brief. Any additional fees necessary to effect the proper and timely filing of this Brief may be charged to Deposit Account No. 26-0090.

Respectfully submitted,

Jim Zegeer

Jim Zegeer, Reg. No. 18,957
Attorney for Appellants

Suite 108
801 North Pitt Street
Alexandria, VA 22314
Telephone: 703-684-8333

Date: August 31, 2006

Atty. Docket No.: 3175-Z

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Laung-Terng Wang et al. Examiner James C. Kerveros

Application No. 10/086,214 Group Art Unit 2133

Filed: March 27, 2002

For: METHOD AND APPARATUS FOR DIAGNOSING FAILURES IN AN INTEGRATED CIRCUIT USING DESIGN-for-DEBUG (DFD) TECHNIQUES

AMENDED BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the final rejection mailed October 5, 2005 of Claims 85 - 103 of the above-identified application.

I. The Real Party in Interest

The real party in interest is Syntest Technologies, Inc.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of the Claims

Claims 85 - 103 are on appeal.

Claims 1 - 84 have been cancelled.

IV. Status of the Amendments

Amendment filed after final on February 17, 2006 was deemed to be non-compliant because the remarks section did not begin on a separate sheet entitled "Remarks/Arguments." A fully compliant amendment is filed herewith.

V. Summary of the Claimed Subject Matter

The present invention is mainly for debugging or diagnosing two or more scan cores and the invention debugs or diagnoses "at-speed" delay faults, so each scan clock must comprise two system clock cycles, whereas to debug/diagnose stuck-type delay faults, each scan clock can comprise only one clock cycle. Thus, applicants' invention uses the term "selected fault type" that allows the DFD circuitry to generate required clock cycles -- "an ordered sequence of capture clocks."

Figure 7A shows the scan clock generator 302 which is composed of clock phase generator 701 and scan clock controller 702. The clock phase generator 701 takes TCK as input and generates three non-overlapping clocks TCK1 706, TCK2 707, and TCK3 708 which have the same frequency as TCK. In addition to the non-overlapping TCK clock signals, the scan clock controller 702 has one or more set of clock input signals shown in Fig. 7A and which are system clocks derived from the outside of the circuit under debug 212. The Select 3 314 signal, generated based on the fault type and the power limit of the targeted scan cores 208, is used to select TCK 220, the non-overlapping TCK clocks 706 to 708, or the external system clocks 703 to 705 as a scan clock. (See page 23 of the specification).

Figure 7B provides a clocking scheme that can reduce both peak power consumption and average power dissipation. During the capture cycle, clock-domain based signal-capture pulses are applied to diagnose stuck-type faults including stuck-at, bridging, or IDDQ faults. (Paragraph bridging page 23 to 24).

Fig. 7C shows non-overlapping clocks which are used to reduce both peak power consumption and average power dissipation and makes it possible to diagnose non-stuck-type delay faults, including transition (gate-delay), path-delay, memory read/write, or multiple-cycle delay faults. (Page 24, lines 3 -15).

Fig. 7D shows the waveforms for scan clocks which complete overlapping TCK clocks used only when a serial scan chain is deployed. This timing makes it possible to diagnose stuck-type faults, including stuck-at, bridging, or IDDQ faults. (Page 24, lines 16-27).

Fig. 7E shows the waveforms for scan clocks when the Select 3 314 signal represents the value of 3. This timing sequence makes it possible to diagnose non-stuck-type delay faults, including transition (gate-delay), path-delay, memory read/write, or multiple-cycle delay faults. (Page 24, lines 28 to page 25, line 6).

With the advance in deep sub-micron manufacturing, an integrated circuit can now contain 30 to 50 clock domains (or scan cores) each controlled by one scan clock (or system clock). During debug or diagnosis, one can no longer assume that you can test all scan cores simultaneously, because the generated heat and test power could potentially damage the chip. Hence, applicants' invention includes:

> ...a DFD selector for indicating which said scan cores and said selected fault type will be debugged or diagnosed simultaneously... (See claim 85, clause (a).)

In compliance with 37 C.F.R. 21.37(a), last sentence thereof, applicant submits the following:

Claims 85-99 do not contain any means clauses.

The step plus function clauses of Claims 100-102 are identified as follows:

100. A method for debugging or diagnosing selected fault types in scan cores using an embedded DFD (design-for-debug) circuitry (204-207, pages 17 and 25) in an integrated circuit, the integrated circuit containing two or more said scan cores (Figs. 2 and 3, element 208) each having a scan clock (302); said method comprising the steps of:

(a) issuing a DBG_SCAN command (Fig. 16 - 1606) for generating a scan debug mode to control said DFD circuitry in said scan cores;

(b) issuing a SELECT command (Fig 16 - 1602) for shifting in selected scan cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said scan cores;

(c) issuing a first SHIFT command (Fig. 16 - 1603) or a first plurality of SHIFT_CHAIN commands for shifting in a predetermined scan pattern to all scan cells within selected scan chains in said scan cores for diagnosis;

(d) issuing one or more CAPTURE commands (Fig. 16 - 1604) for capturing output responses into all said scan cells in said scan cores;

(e) issuing a second SHIFT command (Fig. 16 - 1605) or a second plurality of SHIFT_CHAIN commands for shifting a new predetermined scan pattern into and output response out of all said scan cells within said selected scan chains in said scan cores for diagnosis;

(f) repeating steps of (d)-(e) (Fig. 16 - 1606) until scan diagnosis is done; and

(g) issuing a STOP command (Fig. 16 - 1607) for generating a stop control signal to stop the scan operation.

101. The method of claim 100, further comprising providing a central DFD controller (Fig. 2, element 203, page 17, line 20) for accepting said commands and generating said scan debug mode and said stop control signal to control said DFD circuitry; wherein said DFD controller interfaces with said DFD circuitry and a TAP (test access port) controller (202, page 17, line 28) in said integrated circuit; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard.

102. The method of claim 100, wherein said faults chosen by said selected fault type in said selected scan core for debug or diagnosis further comprise selectively stuck-type faults or non-stuck-type delay faults; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults. (Figs. 7B-7E, page 23, line 27 to page 25, line 6).

VI. Grounds of Rejection to be Reviewed on Appeal

1. The final rejection of claims 85-87, 89-93, 99 under 35 U.S.C. §102(e) as being anticipated by Swamy (US Patent No. 6,686,759) (hereinafter "Swamy").

2. The final rejection of claim 88 under 35 U.S.C. §103(a) as being unpatentable over Swamy (US Patent No. 6,686,759) (hereinafter "Swamy").

3. The final rejection of claims 94-98 under 35 U.S.C. §103(a) as being unpatentable over Swamy (U.S. Patent No. 6,686,759) (hereinafter "Swamy") in view of McLaurin et al (U.S. Patent No. 6,598,192) (hereinafter "McLaurin").

4. The final rejection of claims 100-103 under 35 U.S.C. §103(a) as being unpatentable over Kim (U.S. Patent No. 6,122,762) (hereinafter "Kim") in view of Swamy (U.S. Patent No. 6,686,759) (hereinafter "Swamy").

VII. Argument

Ground No. 1

In regard to the Swamy patent, in attempting to read the Swamy patent on applicants' claim 85, the Examiner contends that Swamy discloses:

> ...a DFD selector (multiplexer 62) having a plurality of inputs (TDO-1, TDO-2, TDO-3... connected to the internal circuit blocks (45-1, 45-2, 45-3...), and outputting a Test Data Output (TDO) signal 66 provided by IEEE Standard 1149.1 TAP 60, for debugging scan cores (46-1, 46-2, 46-3....) with their fault types.
> (Page 3 of the Final Rejection).

This is not the case. Swamy's Fig. 2 discloses a circuit in which the inputs to the scan core's 46-1, 46-2, 46-3... are controlled by the demultiplexer 52 which outputs clock signals TCK-1, TCK-2, TCK-3... TCK-2_n to the cores selected by select register 56. The select register 56 also selects the corresponding outputs TDO-1, TDO-2, TDO-3...TDO-2_n inputs to the multiplexer 62 which are the test outputs from the scan cores 45-1, 45-2, 45-3, etc. Thus, the demultiplexer 52, select register 56 and multiplexer 62 assures that when a test clock TCK-1, for example, is applied to scan block circuit cores 45-1 that the output from that block TDO-1 is outputted from the multiplexer at the proper time. (Swamy, col. 7, lines 17 *et seq*). It has nothing to do with applicants' invention which involves a DFD selector indicating which sets of scan core and faults types will be debugged or diagnosed simultaneously. The Swamy reference says nothing about fault types. In fact, the term "fault" does not appear in the Swamy specification.

In essence, what the Examiner has done in attempting to read applicants' claim 85 on the Swamy reference is to pick out bits and pieces, from the reference and assign functions to them for which there is no reasonable basis. Moreover, in seeking to read applicants' claim 85 on the Swamy reference, the Examiner has reversed the order of the Swamy parts and their function.

Whereas applicants' claim 85 calls for a DFD selector for indicating which scan cores and selected fault types will be debugged or diagnosed simultaneously, note the Swamy reference is silent.

Whereas applicants' claim 85 calls for a multiplexer for connecting the DFD selector and the scan connector to a TAP (test access port) controller in the integrated circuit. Swamy uses his demultiplexer 52 and multiplexer 62 with an input register to select the demultiplexer clock output and assure that the multiplexer test data output are synchronized.

Applicants' claim 86 calls for a scan debug mode wherein the scan debug mode is set to a logic value 1 when the scan cores are to be diagnosed and set to a logic value 0 when the scan cores are not to be diagnosed. At column 7, line 60 *et seq*, Swamy states:

> The rest of the signals, Test Data Input 68, Test Mode Select 70, and Test Reset 72 are common to all the test access ports 60, and are preferably connected directly to their respective chip-level pins.

Nothing corresponding to the function recited in claim 86 is set out in this portion of the Swamy disclosure.

Claim 87 recites that the:

> ...TAP controller is constructed according to a selected Boundary-scan Standard which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out), TCK (test clock), TMS (test mode select), and selectively TRSTB (test reset)

which, as shown above, does not find a response in Swamy. Claim 89 depends from claim 87 and further restricts the DFD selector to shift register for two or more bits in each said scan core to indicate whether said scan core will be diagnosed and what said selected fault type shall be targeted which, as shown above, is not disclosed or suggested in the Swamy disclosure. Clearly, Swamy does not target any fault type in particular and does not seek to

control which scan cores and which selected fault types will be debugged or diagnosed simultaneously.

Claims 90-92 depend from claim 87 and relate to the use of a plurality of multiplexers to stitch multiple scan chains together either as a serial scan chain or as multiple scan chains to share the same scan clock together. No such teaching or suggestion is shown in the Swamy reference. Claim 93 depends from claim 85 and specifies the scan connector further comprises selectively inserting an inverter and a lock-up element between any two multiple scan chains when stitched together to form a serial scan chain or a grouped scan chain wherein the lock-up element is selected from a D latch or D flip-flop. The terms "D latch" or "D flip-flop" do not even appear in the Swamy disclosure.

Ground No. 2

The rejection of claim 88 under 35 U.S.C. 103(a) as being unpatentable over Swamy is clearly in error. Again, Swamy does not even mention fault types and as explained above, applicants use the term "selected fault type" to allow the DFD circuitry to generate the required ordered sequence of capture clock. No teaching or suggestion is found in the Swamy disclosure. While it may be true as the Examiner says that it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate various fault conditions, it was not known in the art to indicate which scan cores and selected fault types "will be debugged or diagnosed simultaneously."

Ground No. 3

The rejection of claims 94-98 under 35 U.S.C. 103(a) as being unpatentable over Swamy in view of McLaurin et al (US 6,598,192) (hereinafter "McLaurin") is clearly in error. As shown extensively above, McLaurin neither discloses nor suggests a scan clock generator for generating an ordered sequence of capture clocks for connection to the scan clocks in the scan cores. Claim 94 characterizes the scan clock generator as comprising a clock phase generator and a scan clock controller. (See Fig. 7(a), sheet 1, and the ordered sequence of capture clock as shown in Figs. 7(b), 7(c), 7(d) and 7(e).) As stated in the paragraph bridging pages 23 and 24:

> ... As illustrated by pulses 733 to 735, this clocking scheme can reduce both peak power consumption and average power dissipation. During the capture cycle, clock-domain based signal-capture pulses 736 to 738 are applied at the frequency of TCK. This makes it possible to diagnose stuck-type faults, including stuck-at, bridging, or IDDQ faults.

No such teaching or suggestion is found in these references or any combination thereof.

Ground No. 4

The rejection of claims 100-103 under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,122,762) in view of Swamy is clearly in error.

Kim does not teach or suggest how to test "two or more" scan cores. As noted earlier, the present invention is mainly for simultaneously debugging or diagnosing two or more selected scan cores for selected fault types.

Claim 100 requires in step (c):

> ...issuing a first SHIFT command or a first plurality of SHIFT_CHAIN commands for shifting in a predetermined scan pattern to all scan cells within selected scan chains in said scan cores for diagnosis;

and in step (e):

> ...issuing a second SHIFT command or a second plurality of SHIFT_CHAIN commands for shifting a new predetermined scan pattern into and output response out of all said scan cells within said selected scan chains in said scan cores for diagnosis;

Neither Kim nor Swamy discloses or teaches how to provide such fault type detection in order for the debug operation.

It is required to provide a DFD selector to indicate which scan cores should be or should not be tested and for which actual fault should be detected simultaneously. This is reflected in claim 100 which recites:

> ...issuing a SELECT command for shifting in selected scan cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said scan cores;

It is not understood how the Examiner can read this language on Kim when the Examiner acknowledges that "Kim fails to disclose, 'two or more scan cores each having a scan clock in an integrated circuit'." With integrated circuits containing 30 to 50 clock domains and it being impractical to test all scan cores simultaneously, applicants have shown how to test successfully selected scan cores and selected fault types simultaneously without exceeding power limitations.

This is not taught or suggested by Kim and not taught or suggested by Swamy for the reasons given earlier herein.

Claims 101-103 depend from claim 100 and are patentable for the same reasons.

CONCLUSION

In conclusion, the Examiner has erred in rejecting the claims and should be reversed.

Respectfully submitted,

Jim Zegeer, Reg. No. 18,957
Attorney for Appellant

Attachments: VIII. CLAIMS APPENDIX (Claims on appeal)
IX. EVIDENCE APPENDIX
X. RELATED PROCEEDINGS APPENDIX

Suite 108
801 North Pitt Street
Alexandria, VA 22314
Telephone: 703-684-8333

Date: August 31, 2006

In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090 along with any other additional fees which may be required with respect to this paper.

VIII. CLAIMS APPENDIX

85. An apparatus for inserting a DFD (design-for-debug) circuitry in an integrated circuit to debug or diagnose selected fault types in scan cores, the integrated circuit containing two or more said scan cores each having a scan clock; said apparatus comprising:

(a) a DFD selector for indicating which said scan cores and said selected fault types will be debugged or diagnosed simultaneously;

(b) a scan connector for connecting multiple scan chains in said scan cores to a boundary-scan chain in said integrated circuit;

(c) a scan clock generator for generating an ordered sequence of capture clocks for connection to said scan clocks in said scan cores; and

(d) a multiplexer for connecting said DFD selector and said scan connector to a TAP (test access port) controller in said integrated circuit.

86. The apparatus of claim 85, further comprising a scan debug mode; wherein said scan debug mode is set to logic value 1 when said scan cores are to be diagnosed, and set to logic value 0 when said scan cores are not to be diagnosed;

87. The apparatus of claim 86, wherein said scan debug mode is generated by a central DFD controller; wherein said central DFD controller interfaces with said TAP controller and said DFD circuitry; and wherein said TAP controller is constructed according

to a selected Boundary-scan Standard which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out), TCK (test clock), TMS (test mode select), and selectively TRSTB (test reset).

88. The apparatus of claim 85, wherein said faults chosen by said selected fault types further comprise stuck-type faults and non-stuck-type delay faults; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ (IDD quiescent current) faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

89. The apparatus of claim 87, wherein said DFD selector further comprises using a shift register of 2 or more bits in each said scan core to indicate whether said scan core will be diagnosed and what said selected fault type shall be targeted; wherein said shift register is controlled by said TCK and its scan data input and scan data output are connected to said TDI and said TDO via said multiplexer, respectively.

90. The apparatus of claim 87, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and connect its scan data input and scan data output to said TDI and said TDO, respectively; wherein said multiplexers are controlled by said scan debug mode.

91. The apparatus of claim 87, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and insert

said serial scan chain before or after said boundary-scan chain; wherein said multiplexers are controlled by said scan debug mode.

92. The apparatus of claim 87, wherein said scan connector further comprises using a plurality of multiplexers to stitch only those scan cells within all said multiple scan chains which share the same said scan clock together as one single scan chain, called grouped scan chain; wherein said grouped scan chain connects its scan data input and scan data output to said TDI and said TDO, respectively; and wherein said multiplexers are controlled by said scan debug mode.

93. The apparatus of claim 85, wherein said scan connector further comprises selectively inserting an inverter and a lock-up element between any two said multiple scan chains when stitched together to form a serial scan chain or a grouped scan chain; wherein said lock-up element is a selected D latch or D flip-flop.

94. The apparatus of claim 87, wherein said scan clock generator for generating an ordered sequence of capture clocks further comprises a clock phase generator and a scan clock controller.

95. The apparatus of claim 94, wherein said clock phase generator is controlled by said TCK and generates a plurality of non-overlapping TCK clocks; and wherein said scan clock controller is controlled by said selected fault type and connects said capture clocks, comprising said TCK, said non-overlapping TCK clocks, and non-overlapping system clocks, to said scan clocks in said scan cores; wherein said non-overlapping system clocks are generated by

the system clocks external to said integrated circuit or on an ATE (automatic test equipment).

96. The apparatus of claim 95, wherein said non-overlapping TCK clocks are used to debug or diagnose said stuck-type faults, including said stuck-at faults, said bridging faults, and said IDDQ faults, in said scan cores in said integrated circuit.

97. The apparatus of claim 95, wherein said non-overlapping system clocks are used to debug or diagnose said non-stuck-type delay faults, including said transition (gate-delay) faults, said path-delay faults, said memory read/write faults, and said multiple-cycle delay faults, in said scan cores in said integrated circuit.

98. The apparatus of claim 95, wherein said scan clock controller further comprises a generator for generating a global scan enable (GSE) signal to control the shift and capture operations of said multiple scan chains in said scan cores; wherein said generator for generating a global scan enable (GSE) signal is further generated by said TAP controller, including Shift_DR, Capture_DR, and Update_DR, according to said selected Boundary-scan Standard.

99. The apparatus of claim 85, wherein said DFD circuitry is further selected for debugging or diagnosing memory scan cores.

100. A method for debugging or diagnosing selected fault types in scan cores using an embedded DFD (design-for-debug) circuitry in an integrated circuit, the integrated circuit containing two or more said scan cores each having a scan clock; said method comprising the steps of:

(a) issuing a DBG_SCAN command for generating a scan debug mode to control said DFD circuitry in said scan cores;

(b) issuing a SELECT command for shifting in selected scan cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said scan cores;

(c) issuing a first SHIFT command or a first plurality of SHIFT_CHAIN commands for shifting in a predetermined scan pattern to all scan cells within selected scan chains in said scan cores for diagnosis;

(d) issuing one or more CAPTURE commands for capturing output responses into all said scan cells in said scan cores;

(e) issuing a second SHIFT command or a second plurality of SHIFT_CHAIN commands for shifting a new predetermined scan pattern into and output response out of all said scan cells within said selected scan chains in said scan cores for diagnosis;

(f) repeating steps of (d)-(e) until scan diagnosis is done; and

(g) issuing a STOP command for generating a stop control signal to stop the scan operation.

101. The method of claim 100, further comprising providing a central DFD controller for accepting said commands and generating said scan debug mode and said stop control signal to control said DFD circuitry; wherein said DFD controller interfaces with said DFD circuitry and a TAP (test access port) controller in said

integrated circuit; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard.

102. The method of claim 100, wherein said faults chosen by said selected fault type in said selected scan core for debug or diagnosis further comprise selectively stuck-type faults or non-stuck-type delay faults; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

103. The method of claim 100, wherein said commands are further used to debug or diagnose memory scan cores.

IX. EVIDENCE APPENDIX

There is no additional evidence.

X. RELATED PROCEEDINGS APPENDIX

There are no proceedings as mentioned in section (II) above, and accordingly no decisions rendered.